**PRACTICAL 5**

**COMPUTER ORGANISATION AND ARCHITECTURE**

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| **PROGRAM: BTECH SY** | **DIVISION: CSBS** |
| **BATCH: 1** | **DATE OF EXPERIMENT: 23/09/2020** |

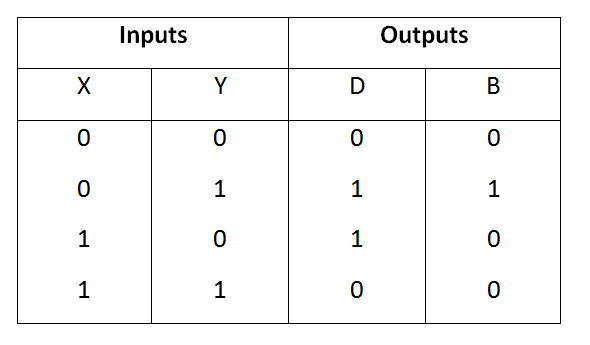
**AIM**

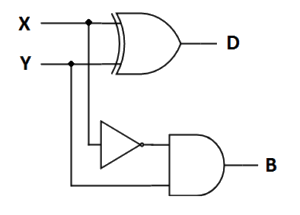
**To Study & Verify Half Subtractor**

**THEORY**

The half-subtractor is a combinational circuit that is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). The logic symbol and truth table are shown below.

  
**Figure-1: Logic Symbol of Half subtractor**

  
**Figure-2: Truth Table of Half subtractor**



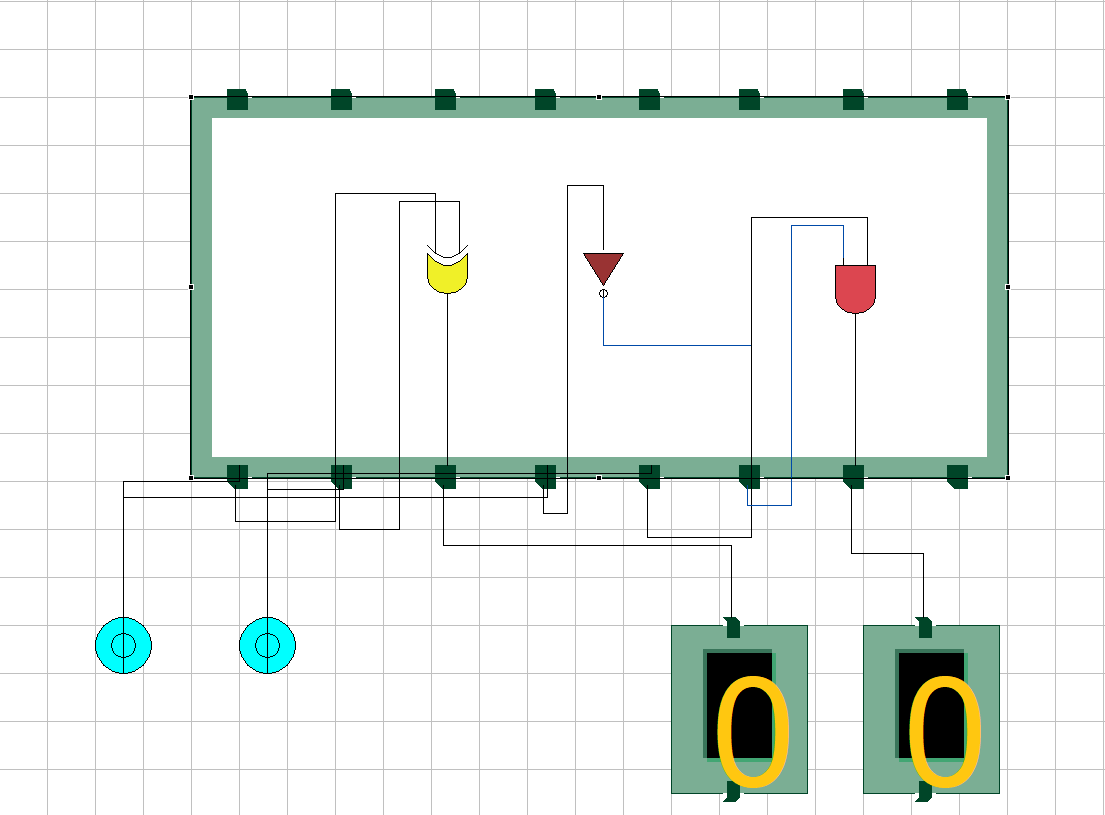
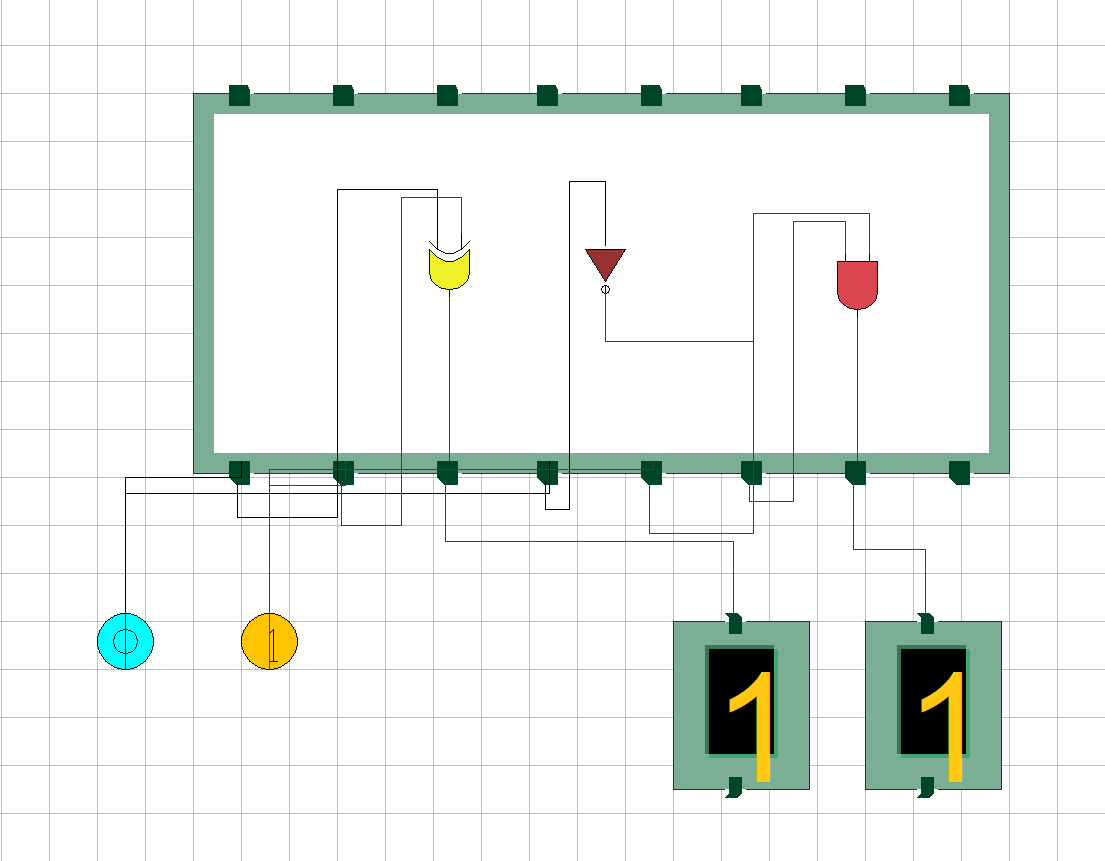
**Figure-3: Circuit Diagram of Half subtractor**

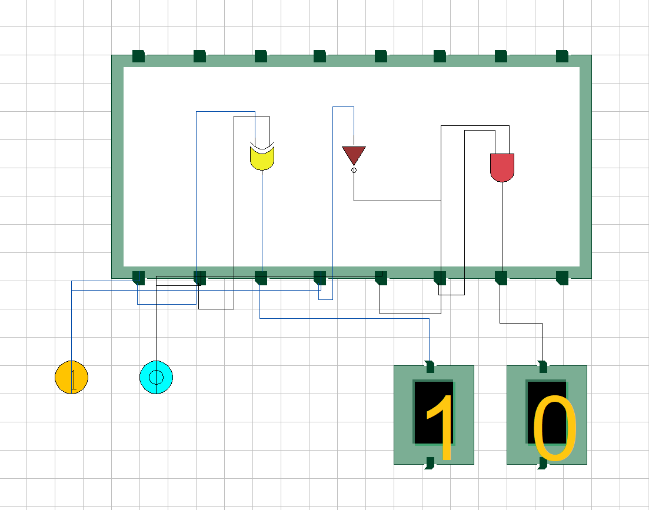
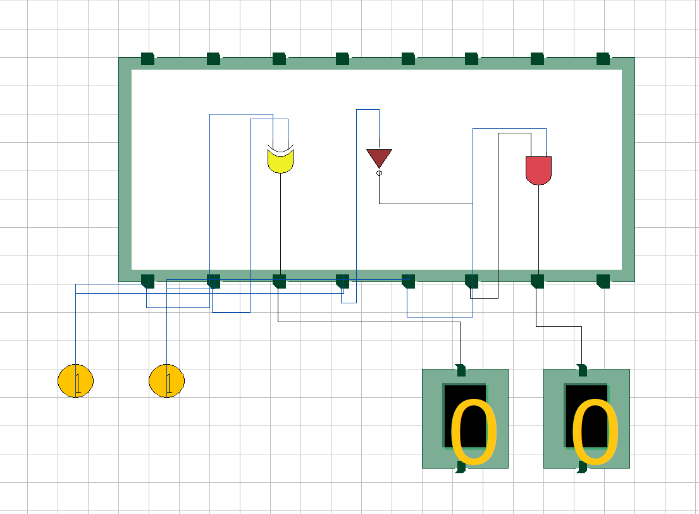
From the above truth table, we can find the Boolean expression.

**D = X ⊕ Y  
B = X' Y**

From the equation, we can draw the half-subtractor circuit as shown in figure 3.

**SIMULATION**

**CONCLUSION**

Hence, we can verify and study the functionality of a half subtractor